CLAIMS

1. A semiconductor device comprising a fuse (3) having a fuse body (3A) and two pads (3Ba, 3Bb) connected by the fuse body (3A) and two conductive layers (5A, 5B) individually connected to two pads (3Ba, 3Bb), the above being formed inside a multilayer structure on a semiconductor substrate (1),

characterized in that a length (L1) of the fuse body (3A) is defined so that the melting location of the fuse (3) becomes positioned in the fuse body (3A) away from a region overlapped on the conductive layers (5A, 5B) when an electrical stress is applied between the two conductive layers (5A, 5B) to melt the fuse (3).

2. A semiconductor device as set forth in claim 1, characterized in that:

the width of the fuse body (3A) is smaller than the width of each of the two pads (3Ba, 3Bb), and

the length (L1) of the fuse body (3A) is 1.8 μm to 20 μm.

3. A semiconductor device as set forth in claim 1, characterized in that at least one of the two conductive layers (5A, 5B) has

a portion of a predetermined width (W3) connected to a corresponding pad (3Ba, 3Bb) and

an interconnect portion having a width narrower

than the portion of the predetermined width (W3).

4. A semiconductor device as set forth in claim 1, characterized in that an interconnect layer having a width narrower than that of the conductive layers (5A, 5B) is connected to at least one of the above two conductive layers (5A, 5B).

5. A semiconductor device as set forth in claim 1, characterized in that, in at least one of the above two conductive layers (5A, 5B), a width (W3) of the portions of the conductive layers (5A, 5B) including the contact regions (4A, 4B) with the pads (3Ba, 3Bb) is 6 μm to 14 μm.

6. A semiconductor device as set forth in claim 1, characterized in that a distance (D0) between the above two conductive layers (5A, 5B) is larger than the distance (L1) between above two pads (3Ba, 3Bb) of the fuse (3).

7. A semiconductor device as set forth in claim 1, characterized in that, in at least one of the above two conductive layers (5A, 5B), a distance (D4) from the contact regions (4A, 4B) connecting the conductive layers (5A, 5B) and the pads (3Ba, 3Bb) to edges of the pad (3Ba, 3Bb) contacting the fuse body (3A) is 0.25 μm to 0.90 μm.

8. A semiconductor device comprising a fuse (3) having a fuse body (3A) and two pads (3Ba, 3Bb) connected by the fuse body (3A) and two conductive layers (5A, 5B) individually connected to two pads (3Ba, 3Bb), the above

being formed inside a multilayer structure on a semiconductor substrate (1),

characterized in that a width (W3) of portions of conductive layers (5A, 5B) including contact regions (4A, 4B) with the pads (3Ba, 3Bb) is defined in at least one of the above two conductive layers (5A, 5B) so that the melting location of the fuse (3) becomes positioned in the fuse body (3A) away from a region overlapped on the conductive layers (5A, 5B) when an electrical stress is applied between the two conductive layers (5A, 5B) to melt the fuse (3).

9. A semiconductor device as set forth in claim 8, characterized in that the width (W3) of the portions of the conductive layers (5A, 5B) including the contact regions (4A, 4B) is 6 μm to 14 μm.

10. A semiconductor device as set forth in claim 8, characterized in that:

the width of the fuse body (3A) is smaller than the width of each of the two pads (3Ba, 3Bb), and

the length (L1) of the fuse body (3A) is 1.8 μm to 20 μm.

11. A semiconductor device as set forth in claim 8, characterized in that at least one of the two conductive layers (5A, 5B) has a portion of a predetermined width (W3) connected to a corresponding pad (3Ba, 3Bb) and an interconnect portion having a width narrower than the

portion of the predetermined width (W3).

12. A semiconductor device as set forth in claim 8, characterized in that an interconnect layer having a width narrower than that of the conductive layers (5A, 5B) is connected to at least one of the above two conductive layers (5A, 5B).

13. A semiconductor device as set forth in claim 8, characterized in that a distance (D0) between the above two conductive layers (5A, 5B) is larger than the distance (L1) between above two pads (3Ba, 3Bb) of the fuse (3).

14. A semiconductor device as set forth in claim 8, characterized in that, in at least one of the above two conductive layers (5A, 5B), a distance (D4) from the contact regions (4A, 4B) connecting the conductive layers (5A, 5B) and the pads (3Ba, 3Bb) to the pad (3Ba, 3Bb) edges contacting the fuse body (3A) is 0.25 μm to 0.90 μm.

15. A semiconductor device comprising a fuse (3) including a conductive material in a multilayer structure on a semiconductor substrate (1), said fuse (3) having a fuse body (3A) and two pads (3Ba, 3Bb) connected by the fuse body (3A),

characterized in that

the width of the fuse body (3A) is smaller than the width of each of the two pads (3Ba, 3Bb), and

the length (L1) of the fuse body (3A) is 1.8 μm

to 20 μm.

16. A semiconductor device comprising a fuse (3) including a conductive material in a multilayer structure on a semiconductor substrate (1), said fuse (3) having a fuse body (3A) and two pads (3Ba, 3Bb) connected by the fuse body (3A), conductive layers (5A, 5B) connected one by one to said two pads (3Ba, 3Bb),

characterized in that, in at least one of the above two conductive layers (5A, 5B), a width (W3) of the portions of the conductive layers (5A, 5B) including the contact regions (4A, 4B) with the pads (3Ba, 3Bb) is 6 μm to 14 μm.

17. A semiconductor device characterized in that:

the semiconductor device has a resistance circuit to which a plurality of unit resistances are connected,

several of said unit resistances have fuses (3, FUSEA, FESEB) connected to them,

each of said fuses (3, FUSEA, FESEB) includes a fuse body (3A) and two pads (3Ba, 3Bb) connected by said fuse body (3A),

said fuses (3, FUSEA, FESEB) and two conductive layers (5A, 5B) connected one to one to said two pads (3Ba, 3Bb) are formed in the multilayer structure on the semiconductor substrate (1),

a length (L1) of each fuse body (3A) is defined so that the melting part of the fuse (3, FUSEA, FESEB) becomes positioned in the fuse body (3A) away from a region overlapped on the conductive layers (5A, 5B) when an electrical stress is applied between the two conductive layers (5A, 5B) to melt the fuse (3, FUSEA, FESEB), and

the combination of the fuses (3, FESEA, FESEB) melting upon application of said electrical stress is selected by an internal circuit (10, 20) to change the resistance value of said resistance circuit.

18. A semiconductor device characterized in that:

the semiconductor device has a resistance circuit to which a plurality of unit resistances are connected,

several of said unit resistances have fuses (3, FUSEA, FESEB) connected to them,

each of said fuses (3, FUSEA, FESEB) is provided with a fuse body (3A) and two pads (3Ba, 3Bb) connected by said fuse body (3A),

said fuses (3, FUSEA, FESEB) and two conductive layers (5A, 5B) connected one to one to said two pads (3Ba, 3Bb) are formed in the multilayer structure on the semiconductor substrate (1),

a width (W3) of portions of conductive layers (5A, 5B) including contact regions (4A, 4B) with the pads

(3Ba, 3Bb) is defined in at least one of the above two conductive layers (5A, 5B) so that the melting part of each of the fuses (3, FESEA, FESEB) becomes positioned in the fuse body (3A) away from a region overlapped on the conductive layers (5A, 5B) when an electrical stress is applied between the two conductive layers (5A, 5B) to melt the fuse (3, FESEA, FESEB), and

the combination of the fuses (3, FESEA, FESEB) melting upon application of said electrical stress is selected by an internal circuit (10, 20) to change the resistance value of said resistance circuit.